NPS1001

0.5 V to 1.8 V, 1.5 A peak, 12 mΩ, load switch

Rev. 1 — 9 December 2024 Product data sheet

1. General description

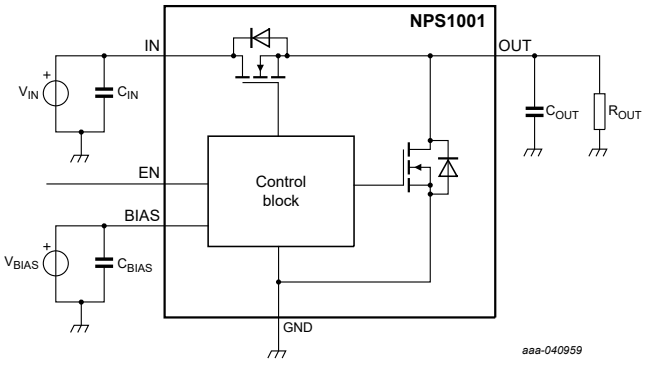
NPS1001 is a low voltage, single-channel load switch with a low $R_{DS,ON}$ (12 mΩ) to minimize IR drop and power loss. It supports up to 0.6 A RMS current and a peak current of 1.5 A.

The switch is controlled by an enable input (EN) which is compatible with 1.2 V logic levels. When the load switch is enabled, the internal switch charges the output capacitor with a controlled inrush current. When the switch is disabled, an 8 Ω on-chip resistor discharges the output to ground and keeps it from floating.

The IC is powered from a separate BIAS pin which is rated for 3 V to 5 V operation.

NPS1001 has an over-temperature protection that latches the device OFF when the internal junction temperature is above the set point ($T_{th(OTLO)}$). At this time, the internal switch is turned off and the output discharge element turns on to discharge the output capacitor. The load switch can be enabled again by toggling the enable (EN) pin.

NPS1001 is available in an ultra-small, space saving, wafer level chip-scale package; 8 bumps; 1.42 mm × 0.72 mm × 0.465 mm body and is characterized for operation over ambient temperature range of –40 °C to 105 °C.



2. Features and benefits

- 0.5 V to 1.8 V operation voltage
- 3 V to 5 V bias voltage
- Low $R_{DS,ON}$: 12 mΩ (typical) at 25 °C, 16 mΩ (maximum) at 85 °C
- Enable logic supports 1.2 V logic levels
- 0.6 A RMS and 1.5 A peak current capability
- Controlled start-up
  - <200 µs from enable to full enhancement of power FET
- Output short tolerant
  - When supplied by a 4.5 A current limited power supply
- Over-temperature shutdown and input UVLO protection
- 8 Ω discharge while disabled
- Small package footprint
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C2a exceeds 500 V
- Specified from T_j = -40 °C to +105 °C

3. Applications

- Mobile phones
- Wearables

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NPS1001UP	-40 °C to +105 °C	WLCSP8	wafer level chip-scale package; 8 bumps; 1.42 × 0.72 × 0.465 mm body	WLCSP8_SOT8068

5. Marking

Table 2. Marking

Type number	Marking code
NPS1001UP	sD

6. Functional diagram

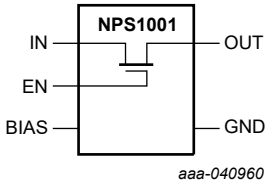


Fig. 1. Logic symbol

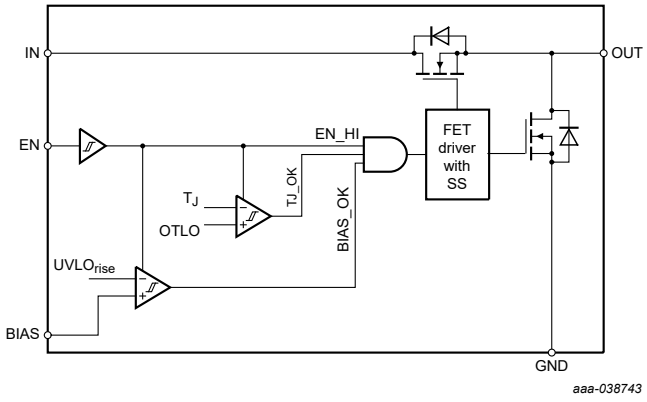


Fig. 2. Functional diagram

7. Pinning information

7.1. Pinning

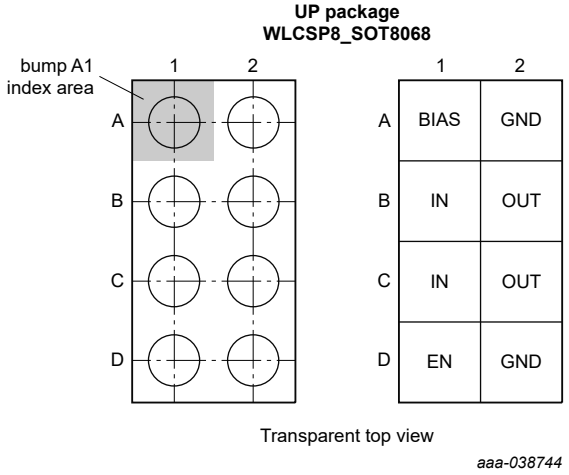


Fig. 3. Bump configuration WLCSP8_SOT8068

7.2. Pin description

Table 3. Pin description

Symbol	Bump	Type	Description
IN	B1, C1	I	Device input. Apply a 0.5 V to 1.8 V voltage source. Bypass with a low ESR capacitor to GND.
OUT	B2, C2	O	Device output. Connect to the load. Bypass with a low ESR capacitor to GND.
BIAS	A1	I	Power supply for the IC. Bypass with a low ESR capacitor to GND. [1]
EN	D1	O	Enable input to the IC. Drive with a 1.2 V logic signal. When EN is high, the main switch is ON and QOD is off, as long as BIAS and temperature are within normal operating ranges. When EN is low, the main switch is turned OFF and QOD is turned ON.
GND	A2, D2	-	Ground (0 V)

[1] This external capacitor is not required under certain cases. See #unique_10 for more information.

8. Functional description

8.1. Overview

The NPS1001 is a load switch with a 11 mΩ N-channel MOSFET designed to operate up to 1.5 A peak current. It is designed for very low inputs of 0.5 V to 1.8 V and the logic input is designed to compatible to 1.2 V logic levels.

The NMOS power FET is placed between the IN and OUT pins and controls the flow of current from IN to OUT. The load switch is powered from the voltage source at the BIAS input and controlled using the EN pin. The OUT pins also have an 8 Ω Quick Output Discharge (QOD) FET internally, which discharges the output to GND when the load switch is OFF and prevents the output from floating. When EN goes high, QOD is turned off and the NMOS power FET is turned on in a controlled manner to control the inrush current.

The IC has a built-in Over Temperature Lock Out (OTLO) that latches off the NMOS when the junction temperature exceeds the OTP threshold. The power FET can be turned back on by toggling the enable (EN) input.

8.2. Operation

The IC is turned-on when the voltage at BIAS pin exceeds the under voltage lockout threshold ($UVLO_{rise}$). Once the voltage at BIAS exceeds $UVLO_{rise}$, the QOD FET is turned ON to pull OUT to ground and the pass-FET is turned off. When a logic high is applied at the EN pin, the IC disables the QOD FET and charges the output capacitance at a controlled slew rate. Once the output voltage is close to the input voltage, the pass FET is turned on completely to achieve low on resistance. Pulling EN low will turn off the pass-FET and turn on the QOD FET to discharge the output capacitor. If at anytime during operation, the junction temperature of the IC exceeds the over temperature set point (T_{OTLO}), the device turns off the pass-FET and turns on the QOD FET. It remains latched in the off-state till the EN pin is toggled externally.

9. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IN}	input voltage	pin IN	–0.3	1.98	V
I_{OUT}	output current	pin OUT	–	1.5	A
V_{BIAS}	input voltage	pin BIAS	–0.3	6.0	V
V_{EN}	input voltage	pin EN	–0.3	6.0	V
T_j	maximum junction temperature	[1]	-40	125	°C
T_{stg}	storage temperature		–65	150	°C

[1] $T_{J(max)}$ internally limited by OTP threshold.

10. ESD ratings

Table 5. ESD ratings

Symbol	Parameter	Conditions	Value	Unit
V_{ESD}	electrostatic discharge voltage	HBM: ANSI/ESDA/JEDEC JS-001 class 2	±2000	V
		CDM: ANSI/ESDA/JEDEC JS-002 class C2a	±500	V

11. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IN}	input voltage	pin IN	0.5	1.8	V
V_{OUT}	output voltage	pin OUT	0.5	1.8	V
V_{BIAS}	input voltage	pin BIAS	3	5.0	V
V_{EN}	input voltage	pin EN [1]	0	5.0	V
T_{amb}	ambient temperature		-40	105	°C

[1] Although the EN pin voltage is rated up to 5 V, the logic high and low voltages need to meet the ON and OFF thresholds stated in the Electrical Characteristics in #unique_17.

12. Recommended components

Table 7. Recommended components

Effective capacitance at output

Symbol	Parameter	Conditions	Min	Max	Unit
C_{OUT}	output capacitance	pin OUT; V_{OUT} = 1.0 V [1]	1	60	µF

[1] see #unique_19

13. Thermal characteristics

Table 8. Thermal information

Measured as per JEDEC standard JESD51-7 on a 4-layer, 1.6 mm FR4 PCB with 2 oz Cu for top and bottom layers and 1 oz Cu for inner layers with no vias. Pads are connected to 0.25 mm copper traces.

Symbol	Parameter	*WLCSP8_SOT8068*	Unit
$R_{\Theta JA}$	junction to ambient thermal resistance	101	°C/W
Ψ_{JT}	junction-to-top characterization parameter	4.1	°C/W

14. Electrical characteristics

Table 9. Electrical characteristics

V_{IN}=1.8 V, V_{BIAS}= 3.4 V, unless otherwise specified. All specs tested in final ATE unless otherwise specified.

Symbol	Parameter	Conditions	T_j = -40 °C to +105 °C			Unit
			Min	Typ[1]	Max	
IN and OUT pins						
$I_{IN(OFF)}$	input leakage current when OFF	V_{IN} = 1.8 V, EN = LO, T_j = -40 °C to +85 °C	-	0.2	6.20	µA
		V_{IN} = 1.8 V, EN = LO, T_j = +25 °C	-	0.34	0.4	µA
		V_{IN} = 1.8 V, EN = LO, T_j = +85 °C	-	3.38	6.20	µA
$I_{IN,Q}$	quiescent current	V_{IN} = 1.8 V, EN = HI, OUT = open	-	0.31	3.50	µA
I_{INRUSH}	inrush current	V_{IN} = 1.8 V, EN goes from low to high, C_{OUT} = 60 µF [2]	-	1.29	1.75	A
BIAS input pin						
$UVLO_{rise}$	BIAS UVLO rising threshold		2.12	2.19	2.26	V
$UVLO_{hys}$	BIAS UVLO hysteresis		-	0.10	-	V
$I_{SH,BIAS}$	BIAS shutdown current	EN = LO, T_j = -40 °C to +85 °C	-	1.06	2.14	µA
		EN = LO, T_j = +25 °C	-	1.06	1.71	µA
		EN = LO, T_j = +85 °C	-	1.22	2.14	µA
$I_{Q,BIAS}$	BIAS quiescent current	EN = HI	-	10	15.1	µA
EN input pin						
$V_{EN,HI}$	EN high threshold	Load switch goes from OFF to ON	0.72	-	-	V
$V_{EN,LO}$	EN low threshold	Load switch goes from ON to OFF	-	-	0.37	V
$V_{EN,HYS}$	EN hysteresis voltage	V_{IN} = 1.0 V, EN = HI, OUT = open	-	77	-	mV
Quick Output Discharge FET (QOD)						
R_{QOD}	quick output discharge FET resistance	V_{OUT} = 1.0 V, EN = LO	-	8	18	Ω
Power FET						
$R_{DS,ON}$	ON-state resistance	V_{BIAS} - V_{OUT} = 1.6 V, I_{OUT} = 1.5 A, T_j = 25 °C	-	12	13	mΩ
		V_{BIAS} - V_{OUT} = 1.6 V, I_{OUT} = 1.5 A, T_j = 85 °C	-	14	16	mΩ
		V_{BIAS} - V_{OUT} = 1.3 V, I_{OUT} = 1.5 A, T_j = 85 °C	-	15	18	mΩ
Over Temperature Protection (OTP)						
T_{OTLO}	over temperature lockout threshold	EN = HI, load switch goes from ON to OFF	115	125	139	°C

[1] Typical numbers are mean values at 25 °C.
[2] Obtained through simulation and characterization, but not tested in production.

15. Dynamic characteristics

Table 10. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);
V_{IN} = 1.8 V, V_{BIAS} = 3.4 V, C_{OUT} = 60 µF unless otherwise specified.
For timing diagrams and test circuit see #unique_23/unique_23_Connect_42_fig_csp_dd1_mzb and #unique_23/unique_23_Connect_42_fig_fnk_dnn_bpb; See also additional graphs in #unique_24 and #unique_25.

Symbol	Parameter	Conditions	T_j = -40 °C to +105 °C			Unit
			Min	Typ[1]	Max	
$t_{d,rise}$	EN rise delay time	EN rising edge to V_{OUT} = 10 %	-	68	-	µs
t_{rise}	output rise time	V_{OUT} rising from 10 % to 90 %	-	157	-	µs
t_{ON}	total turn-on Time	EN rising edge to V_{OUT} = 90 %	-	212	-	µs
T_{ENH}	total time to enhance the power FET	EN rising edge to R_{on} within 10 % of steady state value [2]	-	151	200	µs
$t_{d,fall}$	EN fall delay time	EN falling edge to V_{OUT} = 90 %	-	75	-	µs
t_{fall}	output fall time	V_{OUT} falling from 90 % to 10 %	-	728	-	µs
t_{OFF}	total turn-off time	EN falling edge to V_{OUT} = 10 %	-	800	-	µs
T_{ENL}	total time to turn-off the power FET	EN falling edge to power FET off [3]	-	-	5	µs
$t_{HI,EN}$	enable high pulse width	EN rising edge to EN falling edge	4	-	-	µs
$t_{LO,EN}$	enable LOW pulse width	EN falling edge to EN rising edge	5	-	-	µs

[1] Typical values are measured at T_j = 25 °C.
[2] Tested in test mode
[3] Design guidance for customer.

15.1. Waveforms and test circuit

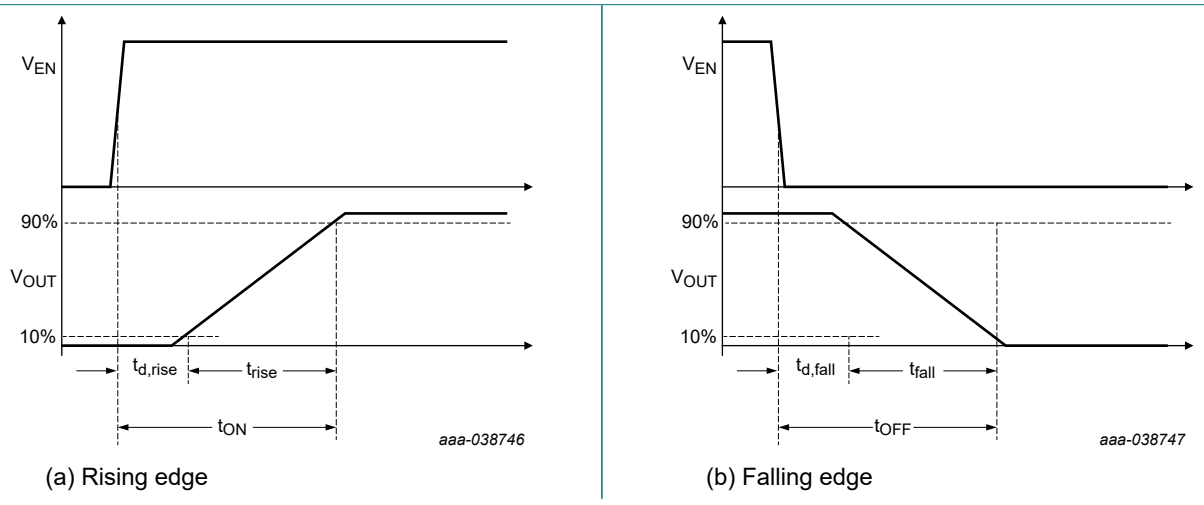
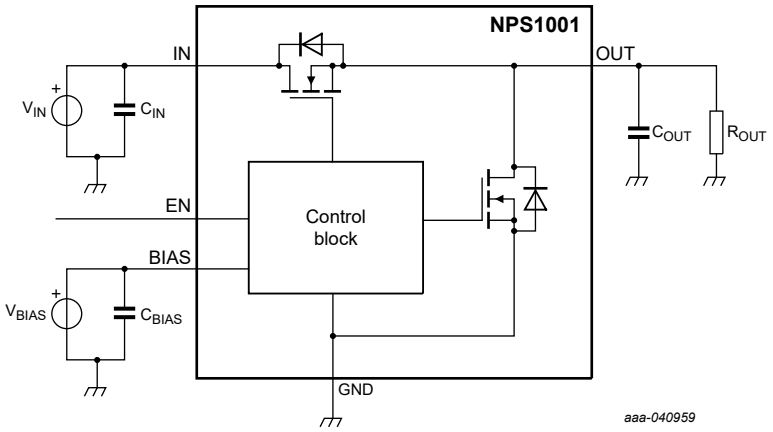


Fig. 4. Timing waveform

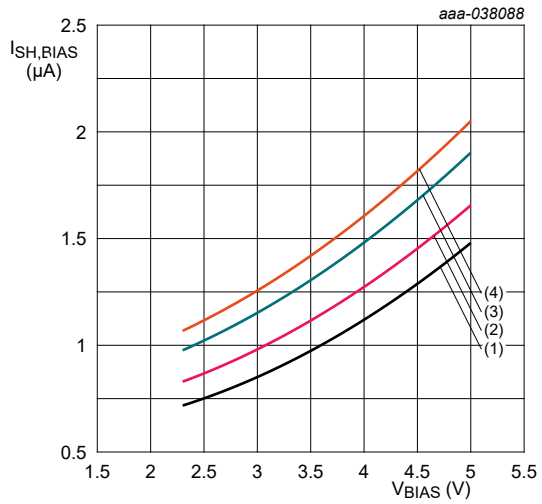


(1) Rise and fall times of the control signal (V_{EN}) are 100 ns.

Fig. 5. Test circuit

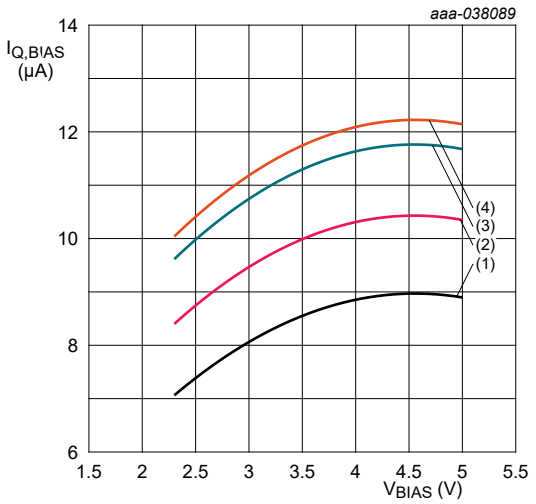
15.2. Typical characteristics

Unless otherwise noted, V_{IN} = 1.0 V, C_{IN} = 1.0 µF, V_{BIAS} = 3.4 V, C_{BIAS} = 0.1 µF, C_{OUT} = 66 µF, R_{OUT} = open



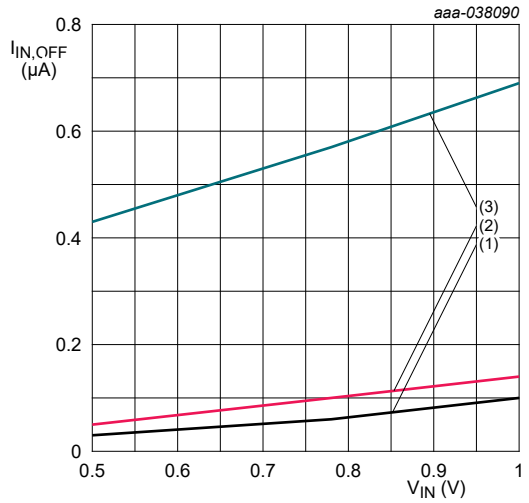
V_{IN} = 1 V; V_{EN} = 0 V
(1) T_j = -40 °C
(2) T_j = 25 °C
(3) T_j = 85 °C
(4) T_j = 105 °C

Fig. 6. Bias shutdown current ($I_{SH,BIAS}$) versus bias voltage



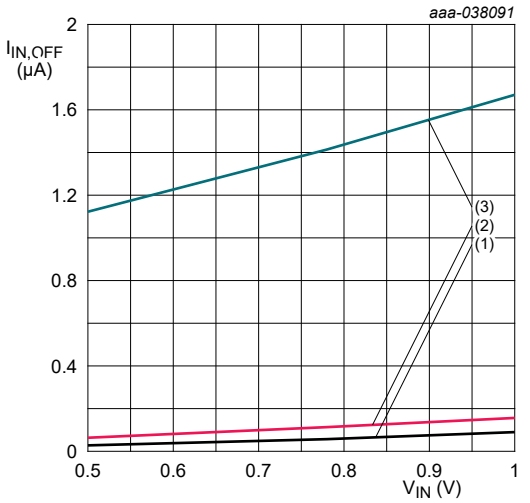
V_{IN} = 1 V; V_{EN} = 1.2 V
(1) T_j = -40 °C
(2) T_j = 25 °C
(3) T_j = 85 °C
(4) T_j = 105 °C

Fig. 7. BIAS quiescent current ($I_{Q,BIAS}$) versus bias voltage



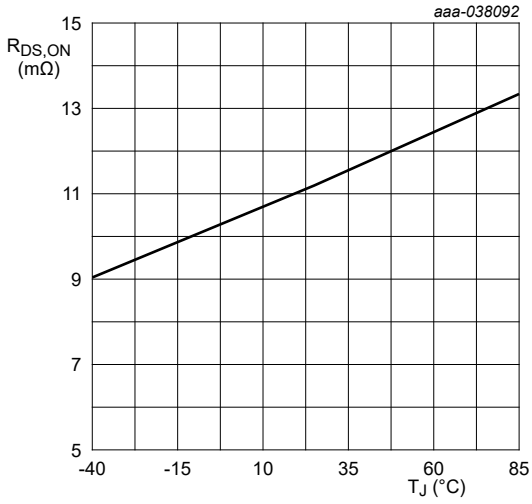
V_{BIAS} = 3.4 V; V_{EN} = 0 V
(1) T_j = -40 °C
(2) T_j = 25 °C
(3) T_j = 85 °C

Fig. 8. Input leakage current ($I_{IN,OFF}$) versus input voltage with EN = LOW



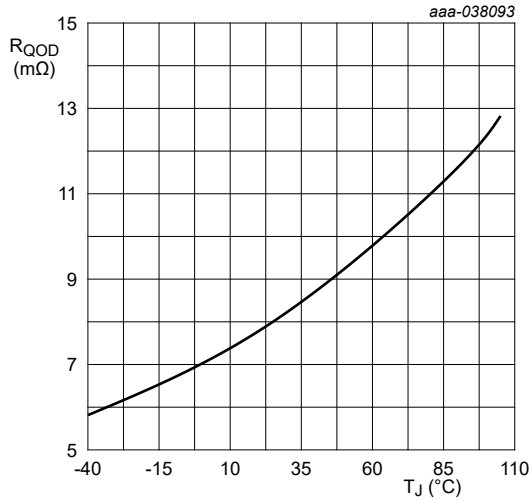
V_{BIAS} = 3.4 V; V_{EN} = 1.2 V
(1) T_j = -40 °C
(2) T_j = 25 °C
(3) T_j = 85 °C

Fig. 9. Input quiescent current ($I_{IN,Q}$) versus input voltage with EN = HIGH



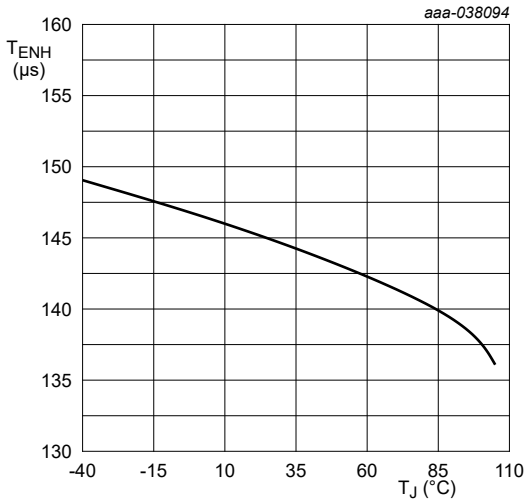
V_{IN} = 1.0 V; V_{BIAS} = 3.4 V

Fig. 10. $R_{DS,ON}$ resistance versus junction temperature



V_{OUT} = 1.0 V; V_{BIAS} = 3.4 V

Fig. 11. R_{QOD} resistance versus junction temperature

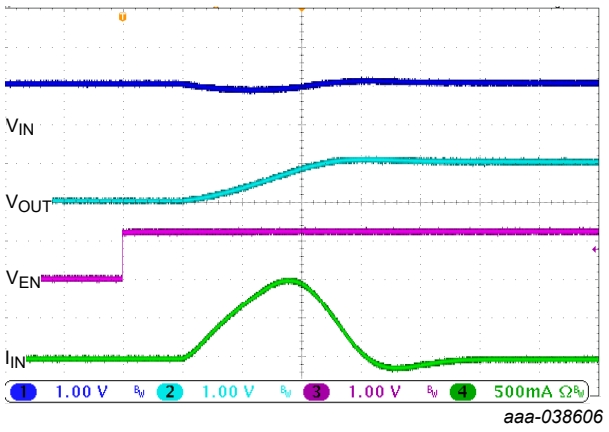


V_{IN} = 1.0 V; V_{BIAS} = 3.4 V

Fig. 12. Enhancement time (T_{ENH}) versus junction temperature

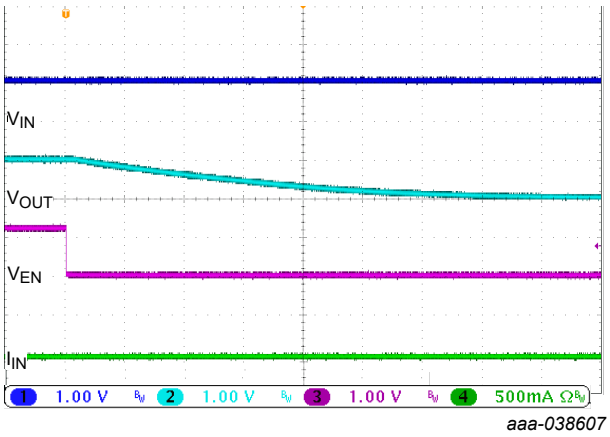
15.3. Typical waveforms

Unless otherwise noted, V_{IN} = 1.0 V, C_{IN} = 1.0 µF, V_{BIAS} = 3.4 V, C_{BIAS} = 0.1 µF, C_{OUT} = 66 µF, R_{OUT} = open.



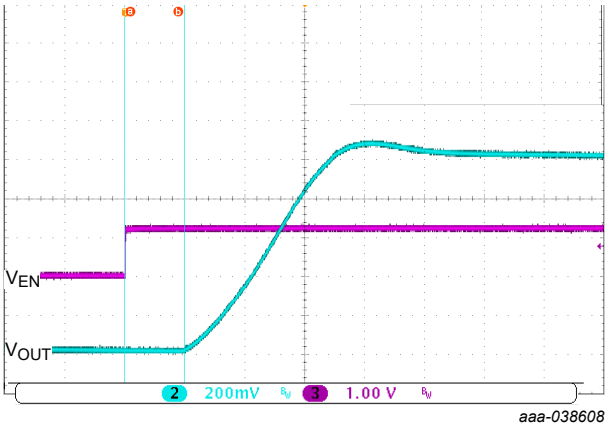
Time scale: 50 µs/div

Fig. 13. Output voltage ramp and inrush current



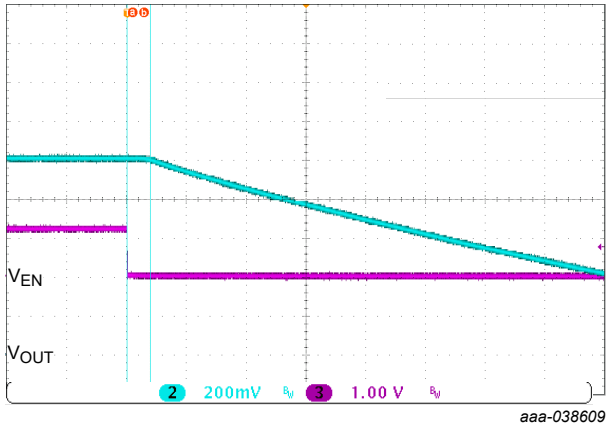
Time scale: 200 µs/div

Fig. 14. Output discharge using QOD FET



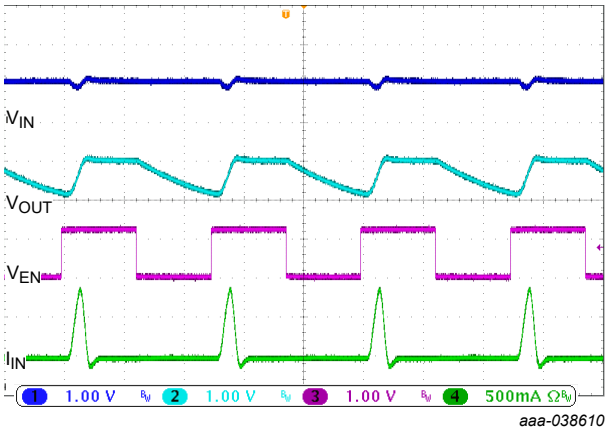
Time scale: 50 µs/div

Fig. 15. Turn-on delay



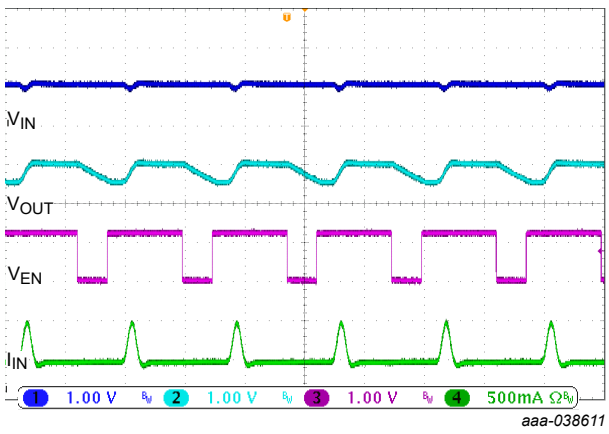
Time scale: 50 µs/div

Fig. 16. Turn-off delay



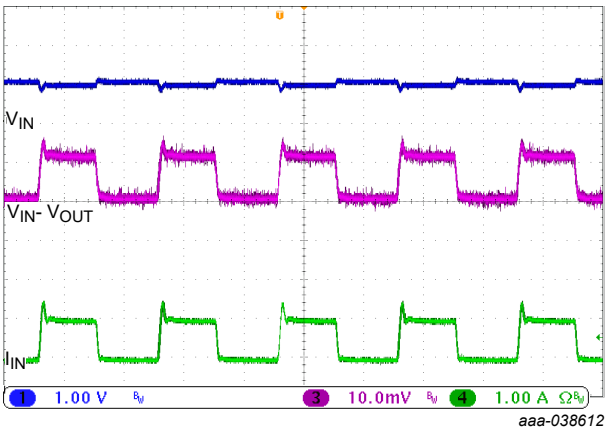
Time scale: 500 µs/div

Fig. 17. EN toggling at 500 µs ON / 500 µs OFF



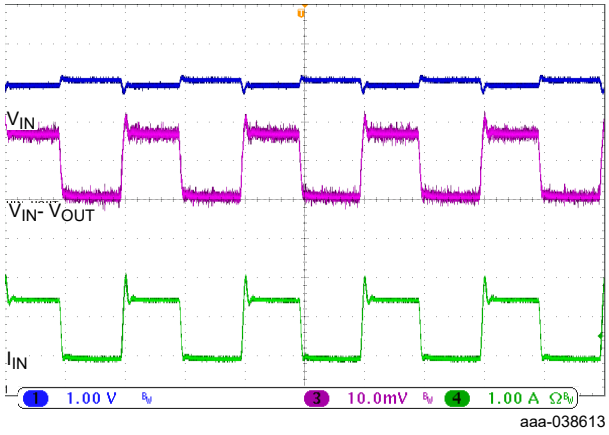
Time scale: 500 µs/div

Fig. 18. EN toggling at 500 µs ON / 200 µs OFF



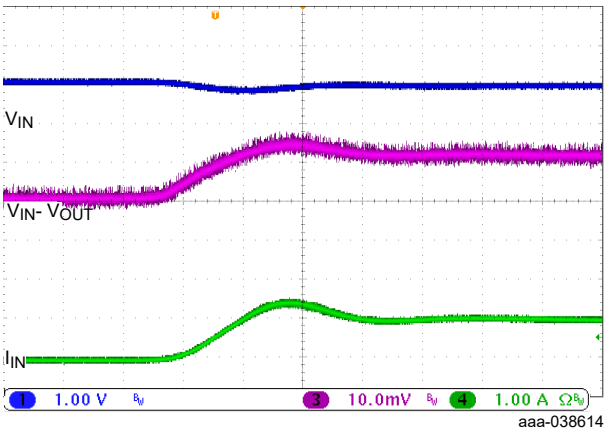
Time scale: 1 ms/div

Fig. 19. Load step response from 0 A to 1 A



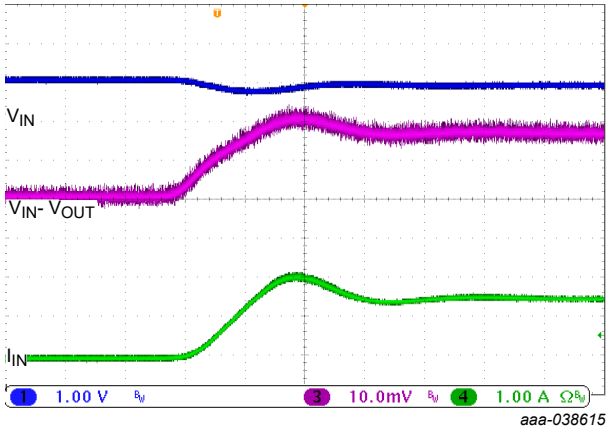
Time scale: 1 ms/div

Fig. 20. Load step response from 0 A to 1.5 A



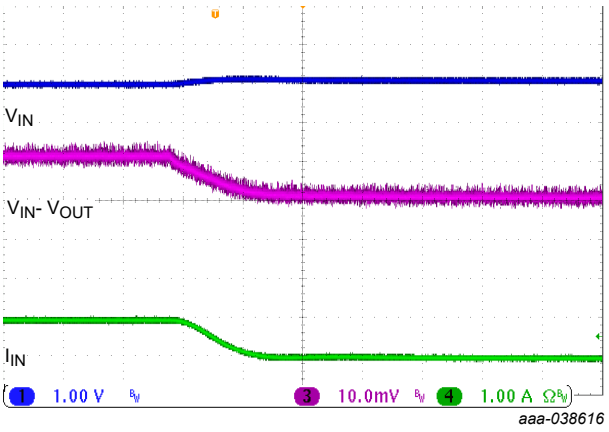
Time scale: 50 µs/div

Fig. 21. Load step response rising edge from 0 A to 1 A



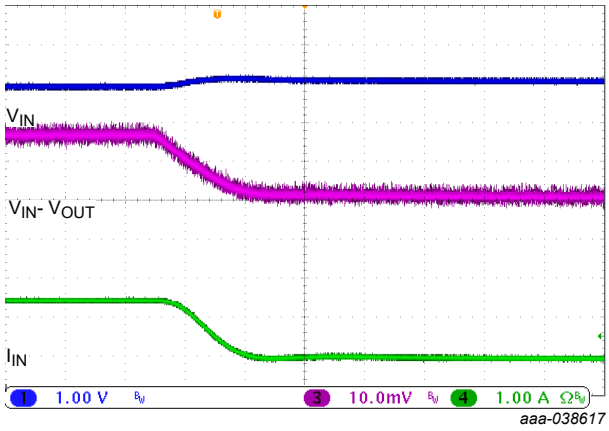
Time scale: 50 µs/div

Fig. 22. Load step response rising edge from 0 A to 1.5 A



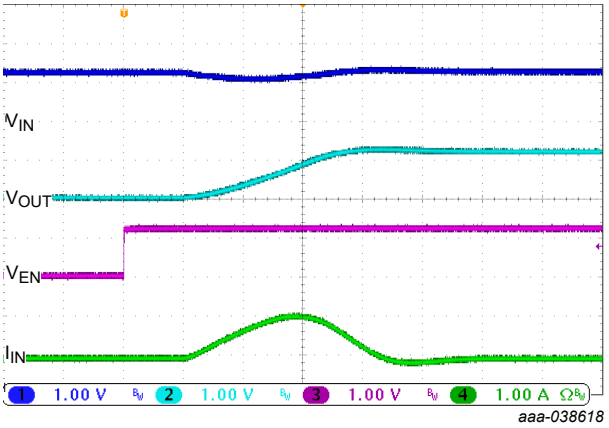
Time scale: 50 µs/div

Fig. 23. Load step response falling edge from 1 A to 0 A



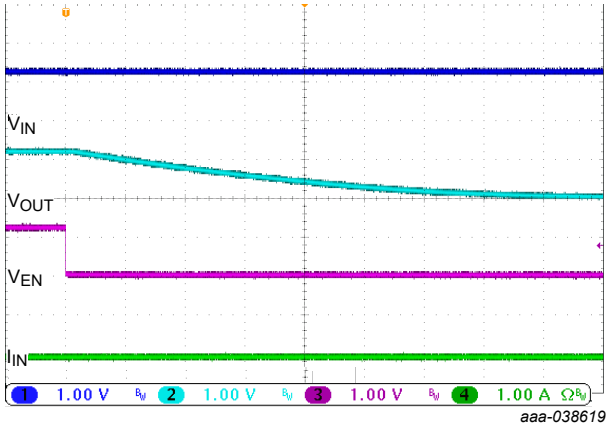
Time scale: 50 µs/div

Fig. 24. Load step response falling edge from 1.5 A to 0 A



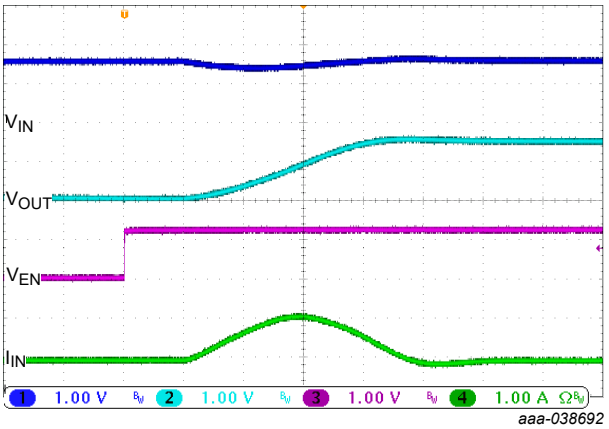
Time scale: 50 µs/div

Fig. 25. Enable at V_{IN} = 1.2 V



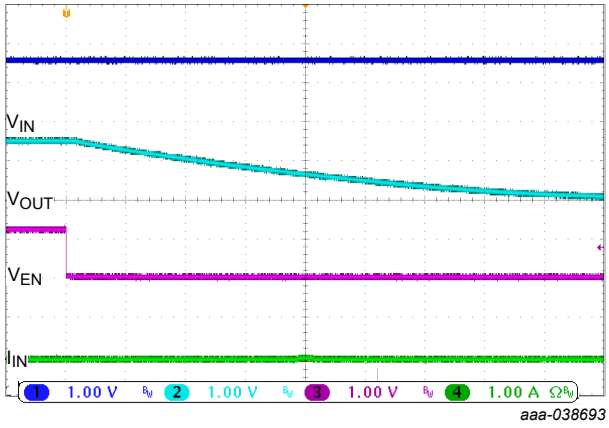
Time scale: 200 µs/div

Fig. 26. Disable at V_{IN} = 1.2 V



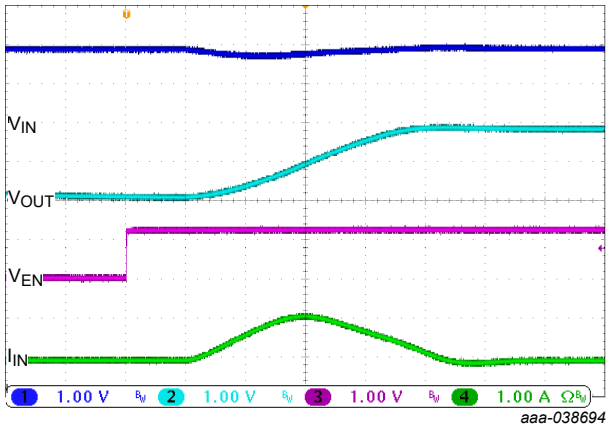
Time scale: 50 µs/div

Fig. 27. Enable at V_{IN} = 1.5 V



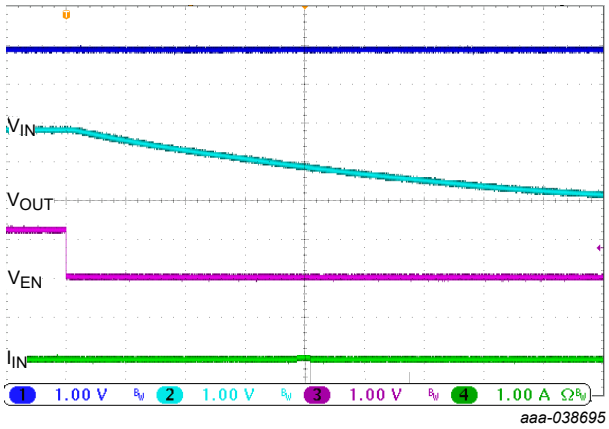
Time scale: 200 µs/div

Fig. 28. Disable at V_{IN} = 1.5 V



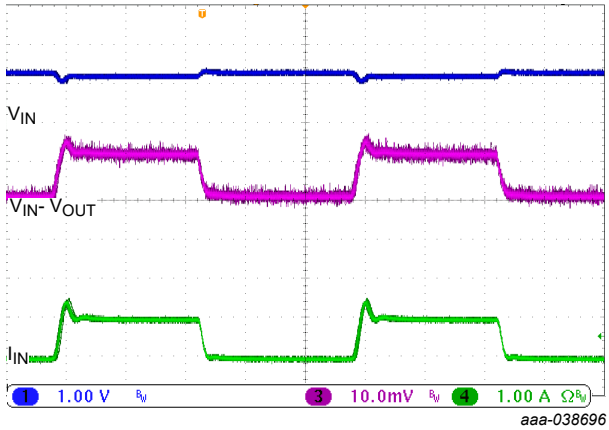
Time scale: 50 µs/div

Fig. 29. Enable at V_{IN} = 1.8 V



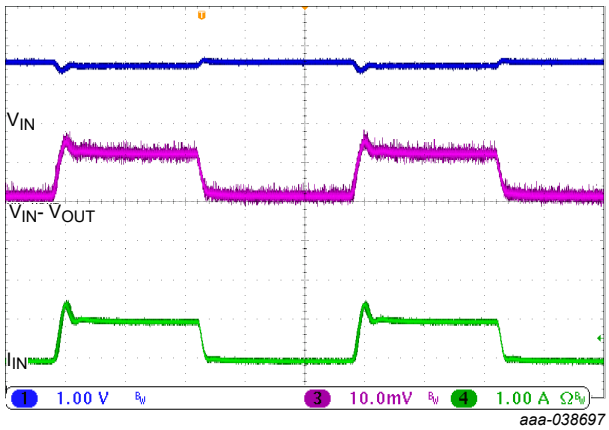
Time scale: 200 µs/div

Fig. 30. Disable at V_{IN} = 1.8 V



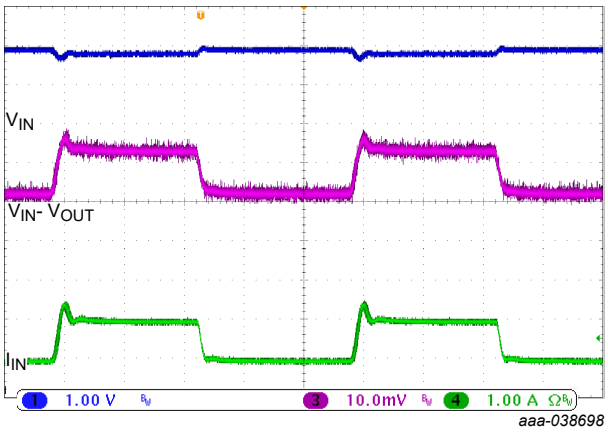
Time scale: 200 µs/div

Fig. 31. Load step response at V_{IN} = 1.2 V



Time scale: 200 µs/div

Fig. 32. Load step response at V_{IN} = 1.5 V



Time scale: 200 µs/div

Fig. 33. Load step response at V_{IN} = 1.8 V

16. Application information

16.1. Capacitor at BIAS pin

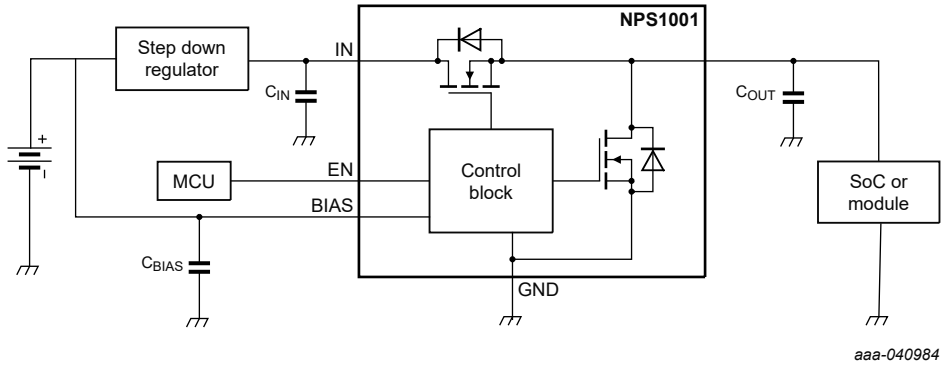
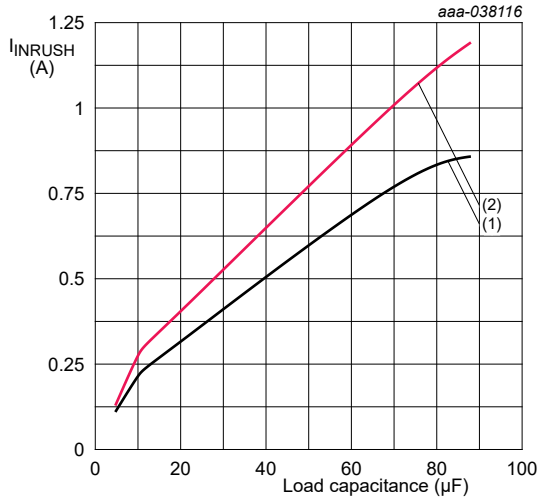


Fig. 34. BIAS power supply

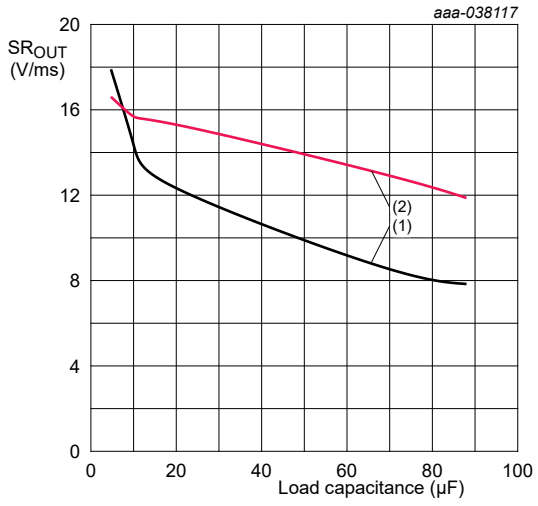
16.2. Inrush current

The NPS1001 does not directly control the inrush current at start-up. Instead, it controls the output slew rate by controlling the slew rate of the gate voltage for the power FET. The pass device acts as a source follower during start-up and the output slew rate follows the slew rate of the pass-FET's gate voltage. The inrush current at any given condition is thus a function of the input voltage and the load capacitance. The following graphs show how the peak inrush current varies with the operating conditions.



V_{BIAS} = 3.4 V
(1) V_{IN} = 0.5 V
(2) V_{IN} = 1.0 V

Fig. 35. Peak inrush current (I_{INRUSH}) versus load capacitance



V_{BIAS} = 3.4 V
(1) V_{IN} = 0.5 V
(2) V_{IN} = 1.0 V

Fig. 36. Output slew rate versus load capacitance

17. Design and assembly recommendations

17.1. PCB design guidelines

For best performance, all traces must be kept as short as possible. The input and output capacitors must be placed close to the device to minimize effects of parasitic trace inductances on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects.

A minimum 1 µF capacitor is recommended from IN to GND as well as OUT to GND, and these should be placed as close to the IC as possible as shown in Section 17.2.

17.2. PCB layout example

A typical layout example if shown in Fig. 37. At least a 2-layer PCB is recommended for best layout practices. The top layer is used for routing the signals as shown in the figure (gray areas are copper planes on the top layer). The bottom layer (or second layer in a multi-layer PCB) is used for a copper plane connected to GND (yellow area). Multiple vias are recommended (number depends on manufacturing guidelines).

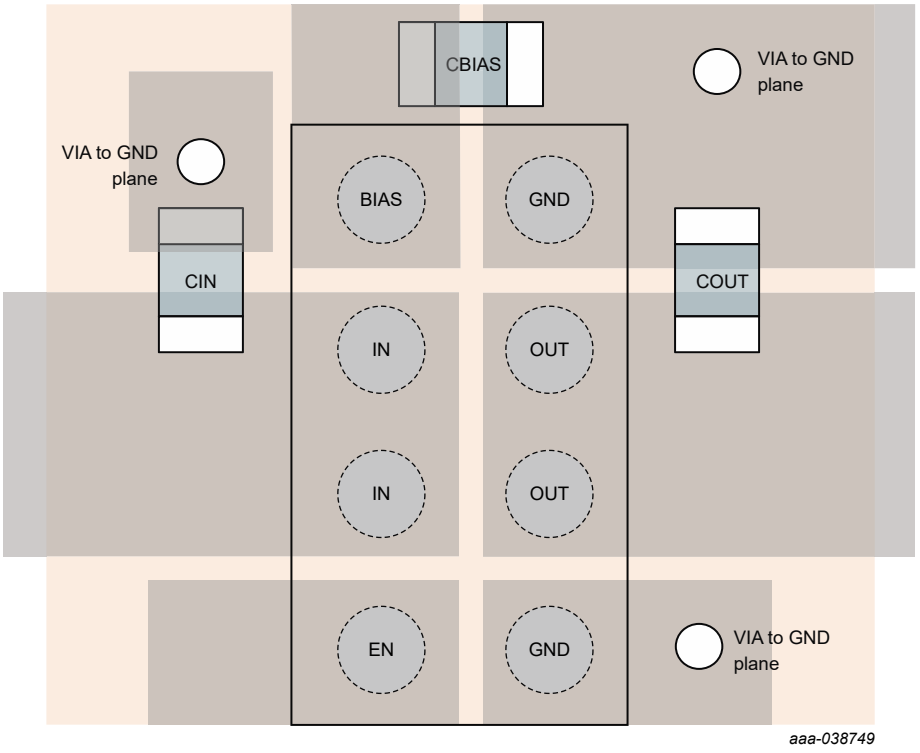
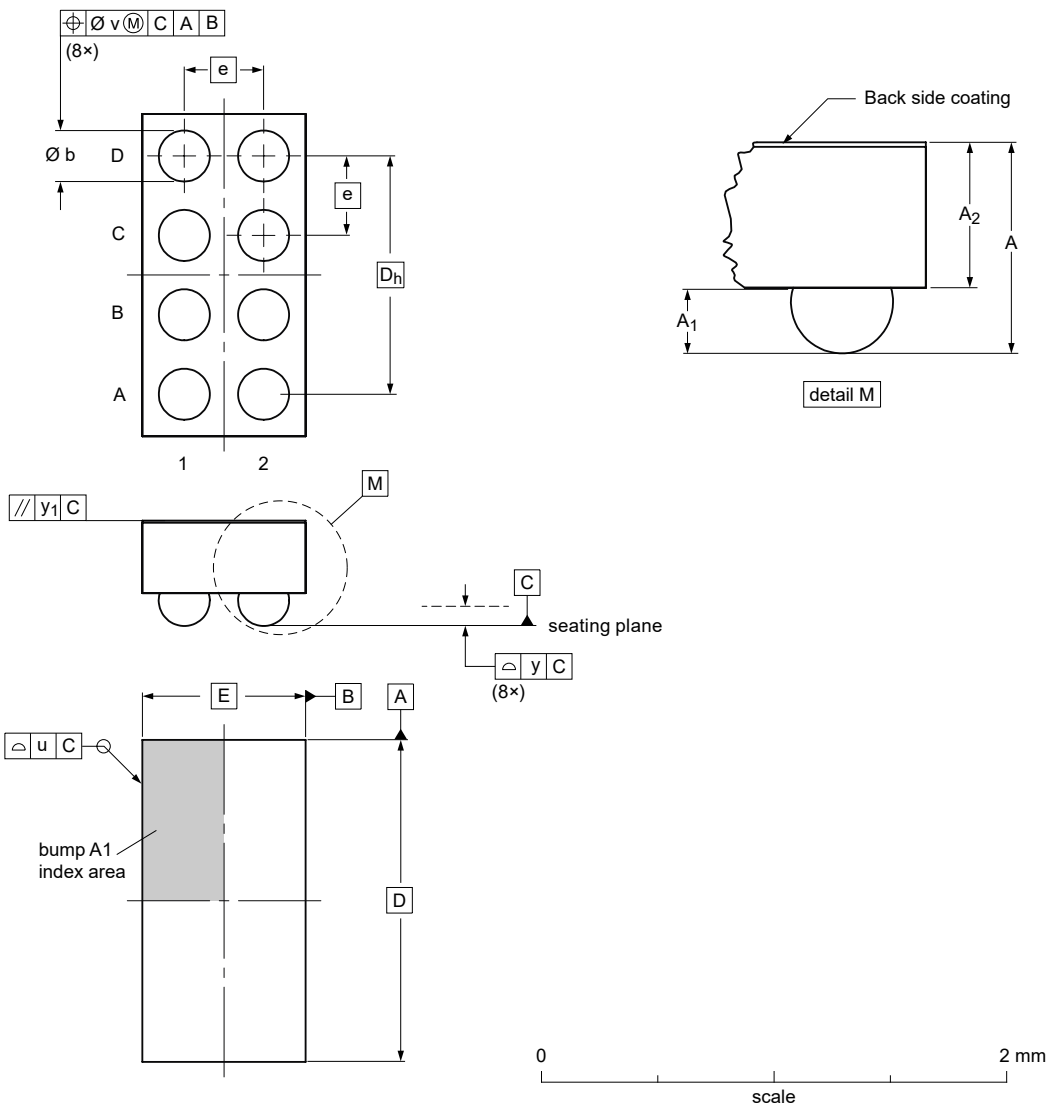


Fig. 37. PCB layout example

18. Package outline

WLCSP8: wafer level chip-scale package; 8 bumps; 1.42 × 0.72 × 0.465 mm body **WLCSP8_SOT8068**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	D_h	E	e	v	u	y	y_1
mm	max	0.465		0.290	0.245	1.42 BSC	1.05 BSC	0.72 BSC	0.35 BSC	0.015	0.03	0.05	0.06
	nom												
	min		0.145	0.240	0.205								

wlcsp8_sot8068_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
WLCSP8_SOT8068						24-01-22

Fig. 38. Package outline WLCSP8_SOT8068 (WLCSP8)

19. Soldering

Footprint information for reflow soldering of WLCSP8 package **WLCSP8_SOT8068**

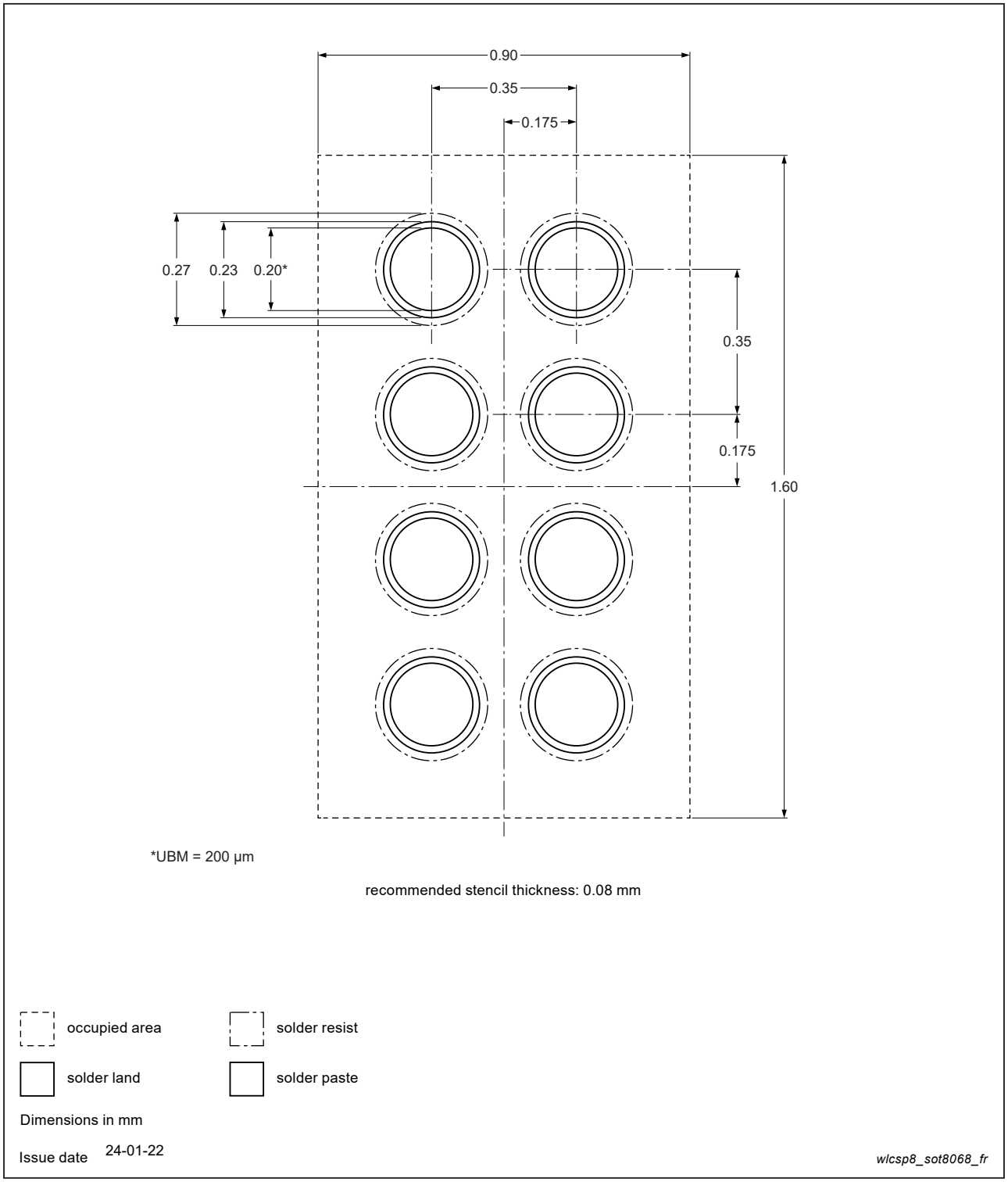


Fig. 39. Reflow soldering footprint WLCSP8_SOT8068 (WLCSP8)

20. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
PCB	Printed-Circuit Board
TTL	Transistor-Transistor Logic

21. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NPS1001 v.1	20241209	Product data sheet	-	-

22. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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